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Pentacene thin-film transistors(TFTs) were fabricated on glass substrates. Aluminum and gold were used for gate and source/drain electrodes. Silicon dioxide was deposited as a gate insulator by PECVD and patterned by reactive ion etching(RIE). The semiconducting pentacene layer was thermally evaporated in vacuum at a pressure of about 10^{-8} Torr and a deposition rate of 0.3 Å/sec. The fabricated devices exhibited the field-effect mobility as large as 0.07 $cm^2/V \cdot sec$, threshold voltage as low as −3.3V, and the on/off current ratio larger than 10^7.

Keywords: Organic thin film transistors; pentacene; evaporation; field-effect mobility; threshold voltage; on-off current ratio

INTRODUCTION

Some organic materials have received considerable attention as materials for the active device applications such as light emitting diodes[1] and TFTs[2]. They

can offer potential advantages in terms of the processing simplicity and manufacturing cost[3]. In this study, pentacene TFTs were fabricated on glass substrates. Aluminum and gold were used for the gate and source/drain electrodes respectively. Silicon dioxide was deposited for the gate insulator by plasma enhancement chemical vapor deposition(PECVD) and etched by RIE for patterning. The operational properties of the fabricated TFTs were characterized by the field-effect mobility, threshold voltage and on/off current ratio.

DEVICES FABRICATION

The schematic cross-section of a pentacene TFT is shown in Figure 1. Aluminum was deposited on the glass substrate by the conventional thermal evaporation, patterned by the lift-off, and annealed. The gate insulator, SiO_2 was deposited by PECVD. The SiO_2 layer was patterned by R.I.E., the thickness of which was about 100 nm. Then, gold was deposited on the gate insulator by the thermal evaporation, whose thickness was 130 nm.

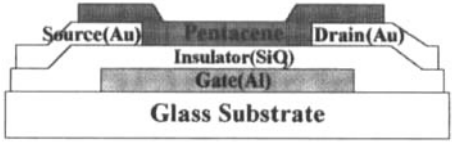

Figure 1. The schematic cross-section of the pentacene TFT fabricated in this study.

RESULT AND DISCUSSION

The transfer characteristics of pentacene TFTs, whose channel lengths are 50, 100, 200, and 250μm respectively, are presented in Figure 2. The channel width of all the devices is 5 mm. The drain bias was 2 V and the gate bias varied from 0V to −20V for the measurements. The on/off current ratio of those devices is larger than 10^7, which is one of the best data. The mobility and threshold voltage were extracted from the I_D vs. V_G data measured in the saturation regime, based on the equation[4]:

$$I_{DS}=\frac{W}{L}\frac{C_i}{2}\mu(V_G-V_{th})^2$$

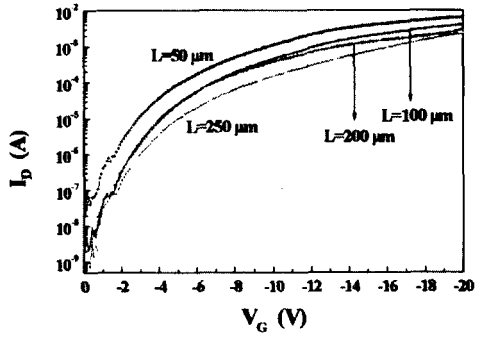

Figure 2. Transfer characteristics of pentacene TFT with gate lengths of 50, 100, 200, 250μm, width of 5 mm (V_D = 2V)

where μ is the field-effect mobility, L and W are the channel length and width, respectively, C_i is the gate capacitance per unit area, and V_{th} is the threshold voltage. V_{th} and μ were extracted from the plot of $I_D^{1/2}$ vs. V_G measured in the saturation regime. The field-effect mobility is as large as 0.07 $cm^2/V\cdot$ sec, which is remarkably high if it is taken account of that the pentacene layer was deposited by the plain thermal. Moreover, V_{th} is as low as –3.30 V, which is one of the lowest turn-on voltages ever reported. The excellent characteristics of the fabricated TFTs are thought to be

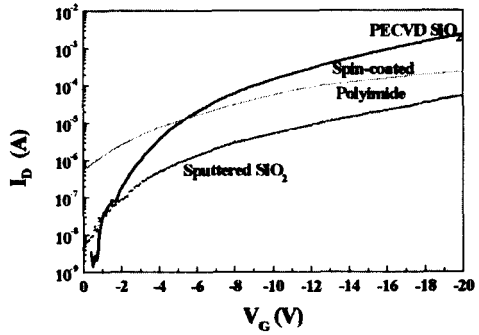

Figure 3. Transfer characteristics of pentacene TFTs with various gate insulators. (L= 50μm, W= 5 mm at V_D = 2V)

attributed to the plasma treatment of the SiO_2 surface during the plasma etching. If an effusion cell is used under lower pressure and the substrate temperature is raised higher, the much better-ordered pentacene layer could be obtained to provide the much improved transistor characteristics that can be comparable to those of amorphous silicon TFTs.

All-organic TFTs can be realized if the SiO_2 is replaced by an organic dielectric medium as a gate insulator with conducting organic electrodes. The spin-coated polyimide layer was used as a gate insulator to build transistors, whose transfer characteristics is presented in Figure 3. Also is provided the transfer characteristics of a pentacene TFT with the gate insulator of sputtered SiO_2. Both TFTs with the polyimide and sputtered SiO_2 exhibited the worse operational properties, which seem to be leaky and incomplete in the channel formation.

CONCULSION

Pentacene TFTs was fabricated on the glass substrate. Aluminum and gold were used for the gate and source/drain electrodes. The SiO_2 was deposited by PECVD and patterned by R.I.E. as a gate insulator. The pentacene layer was thermally evaporated. Electrical characterizations of the TFTs show that the field-effect mobility is as large as 0.07 $cm^2/V\cdot$ sec, on/off current ratio over 10^7, and threshold voltage as low as –3.30 V. If an effusion cell is used under lower pressure and the substrate temperature is raised higher, the much improved transistor characteristics could be obtained.

Acknowledgements

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